

1 3. (Cancelled).

1 4. (Amended) The computer system of Claim 1, wherein the portion of the starting
2 address includes a plurality of most significant bits of the starting address.

1 5. The computer system of Claim 4, wherein execution unit shifts the data elements
2 by a predetermined number of bit positions to obtain the starting address of the cache line in
3 which data is to be invalidated.

1 6. The computer system of Claim 1, wherein the predetermined portion of the
2 plurality of cache lines is a page in the cache memory.

1 7. (Amended) A computer system comprising:
2 a first storage area to store data;
3 a cache memory having a plurality of cache lines each of which stores data;
4 a second storage area to store a data operand containing a portion of an address; and
5 an execution unit coupled to said first storage area, said second storage area, and said
6 cache memory, said execution unit to operate on the portion of an address in said data operand to
7 copy data from a predetermined portion of the plurality of cache lines in the cache memory to
8 the first storage area, in response to receiving a single instruction of a processor instruction set.

1 8. The computer system of claim 7, wherein the data operand is a register location.

1 9. The computer system of claim 8, wherein the register location contains a plurality
2 of most significant bits of a starting address of the cache line in which data is to be copied.

1 10. (Amended) The computer system of claim 9, wherein execution unit shifts the
2 portion of an address by a predetermined number of bit positions to obtain the starting address of
3 the cache line in which data is to be copied.

1 11. The computer system of Claim 7, wherein the predetermined portion of the
2 plurality of cache lines is a page in the cache memory.

1 12. The computer system of Claim 7, wherein the execution unit further invalidates
2 data in the predetermined portion of the plurality of cache lines in response to receiving the
3 single instruction, upon copying the data to the first storage area.

D) 1 13. (Cancelled).

1 14. (Cancelled).

1 15. (Cancelled).

1 16. (Cancelled).

C) 1 17. (Cancelled).

1 18. (Cancelled).

1 19. (Cancelled).

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1 27. (Cancelled).

1 28. (Cancelled).

1 29. (Cancelled).

1 30. (Cancelled).

1 31. (Cancelled).

1 32. (Cancelled).

1 33. (Cancelled).

C 1 34. (Cancelled).

1 35. (Cancelled).

1 36. (Cancelled).

1 37. (Cancelled).

D 1 38. A computer system comprising:
2 a cache memory having a plurality of cache lines each of which stores data;
3 a storage area to store a data operand; and
4 an execution unit coupled to said storage area to operate on data elements in said data
5 operand identifying a user-definable linear or physical address identifying a predetermined
6 portion of the plurality of cache lines to invalidate data in the predetermined portion of the
7 plurality of cache lines in response to receiving a single cache control instruction of a processor
8 instruction set, the single cache control instruction including a reference to the data operand.

1 39. The computer system of Claim 38, wherein the data operand is a register location.

1 40. The computer system of Claim 39, wherein execution unit shifts the data elements
2 by a predetermined number of bit positions to obtain the starting address of the cache line in
3 which data is to be invalidated.

1 41. The computer system of Claim 38, wherein the predetermined portion of the
2 plurality of cache lines is a page in the cache memory.

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1 42. (New) A processor comprising:
2 a decoder configured to decode instructions; and
3 a circuit coupled to said decoder, said circuit in response to a single decoded instruction
4 of a processor instruction set being configured to:
5 [read a portion of an address located in a register specified in the decoded
6 instruction to] obtain a starting address of a predetermined area of a cache memory on
7 which the instruction will be performed; and
8 invalidate in the predetermined area of cache memory.

1 43. (New) The processor of Claim 42, wherein the portion of an address includes a
2 plurality of most significant bits of the starting address.

1 44. (New) The processor of Claim 43, wherein the circuit shifts the portion of an
2 address by a predetermined number of bits positions to obtain the starting address of a cache line
3 of the predetermined area of the cache memory in which data is to be invalidated.

1 45. (New) The processor of Claim 42, wherein the predetermined area of the cache
2 memory comprises a plurality of cache lines forming a page in the cache memory.

1 46. (New) A processor comprising:
2 a decoder to decode instructions, and
3 a circuit coupled to said decoder, said circuit in response to a single decoded instruction
4 of a processor instruction set being configured to:

5 read a portion of an address located in a register specified in the decoded
6 instruction to obtain a starting address of a predetermined area of a cache memory on
7 which the instruction will be performed;
8 copy data in the predetermined area of the cache memory; and
9 store the copied data in storage area separate from the cache memory.

1 47. (New) The processor of Claim 46, wherein the portion of an address includes a
2 plurality of most significant bits of the starting address.

1 48. (New) The processor of Claim 47, wherein the circuit shifts the portion of the
2 address by a predetermined number of bit positions to obtain the starting address of a cache line
3 of the cache memory in which data is to be copied.

1 49. (New) The processor of Claim 47, wherein the predetermined area comprises a
2 plurality of cache lines forming a page in the cache memory.

1 50. (New) The processor of Claim 47, wherein said circuit further invalidates the
2 data in the predetermined portion of the plurality of cache lines in response to receiving the
3 single instruction, upon copying the data to the storage area.

1 51. (New) A computer-implemented method, comprising:
2 a) decoding a single instruction of a processor instruction set;
3 b) in response to said decoding of the single instruction, obtaining a portion of a
4 starting address of a predetermined areas of a cache memory on which the single instruction will
5 be performed by reading a portion of an address contained in a storage location specified in the
6 decoded instruction; and
7 c) completing execution of said single instruction by invalidating data in the
8 predetermined area of the cache memory.

1 52. (New) The method of Claim 51, wherein c) comprises setting an invalid bit
2 corresponding to the predetermined area of the cache memory.

1 53. (New) The method of Claim 51, wherein b) comprises:

2 shifting the portion of the starting address by a predetermined number of bit positions to
3 obtain the starting address of a cache line of the cache memory in which data is to be invalidated.

1 54. (New) The method of Claim 53, wherein the portion of the starting address
2 contains a plurality of most significant bits of the starting address, and the predetermined number
3 of bit positions represent the number of least significant bits of the starting address.

1 55. (New) The method of Claim 51, wherein the predetermined area is a page in the
2 cache memory.

1 56. (New) A computer-implemented method, comprising:

2 a) decoding a single instruction of a processor instruction set;
3 b) in response to said decoding the single instruction, obtaining a portion of a
4 starting address of a predetermined area of a cache memory on which the single instruction will
5 be performed by reading a portion of an address contained in a storage location specified in the
6 decoded instruction; and

7 c) completing execution of said single instruction by copying data in the
8 predetermined area of cache memory and storing the copied data in a storage area separate from
9 the cache memory.

1 57. (New) The method of Claim 56, wherein c) comprises setting an invalid bit
2 corresponding to the predetermined area of the cache memory.

1 58. (New) The method of Claim 56, wherein b) comprises:
2 shifting the portion of the starting address by a predetermined number of bit positions to
3 obtain the starting address of a cache line associated with the predetermined area.

1 59. (New) The method of Claim 58, wherein the portion of the starting address
2 contains a plurality of most significant bits of the starting address, and the predetermined number
3 of bit positions represent the number of least significant bits of the starting address.

1 60. (New) The method of Claim 56, wherein the predetermined area comprises a
2 plurality of cache lines forming a page in the cache memory.

1 61. (New) The method of Claim 56, further comprises:

2 d) invalidating the data in the predetermined area in response to receiving the single
3 instruction, upon copying the data to the storage area.

1 62. (New) A computer-readable apparatus, comprising:

2 a computer-readable medium that stores an instruction which when executed by a
3 processor causes said processor to:

4 a) decode a single instruction of a processor instruction set;

5 b) in response to decoding the single instruction, obtain a portion of a starting
6 address of a predetermined area of a cache memory on which the single instruction will
7 be performed by reading a portion of an address contained in a storage location specified
8 in the decoded instruction; and

9 c) complete execution of said single instruction by invalidating data in the
10 predetermined area of the cache memory.

1 63. (New) A computer-readable apparatus comprising:

2 a computer-readable medium that stores an instruction which when executed by a
3 processor causes said processor to:

4 a) decode a single instruction of a processor instruction set;

5 b) in response to decoding the single instruction, obtain a portion of a starting
6 address of a predetermined area of a cache memory on which the single instruction will
7 be performed by reading a portion of an address contained in a storage location specified
8 in the decoded single instruction; and

9 c) complete execution of said single instruction by copying data in the
10 predetermined area of the cache memory and storing the copied data in a storage area
11 separate from the cache memory.

1 64. (New) The apparatus of Claim 63, wherein the instruction further causes the

2 processor to:

3 invalidate the data in a predetermined portion of a plurality of cache lines forming the
4 predetermined area of the cache memory in response to receiving the instruction, upon copying
5 the data to the storage area.